What is claimed is:

1. A decoder system, comprising:

a State Metric Update unit including a state metric memory and a cascaded Add/Compare/Select (ACS) unit,

wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory,

wherein an ACS stage is operable to identify a plurality of path decisions and communicate the identified path decisions to a next ACS stage coupled thereto; and

a Traceback unit for storing a set of accumulated path decisions in a traceback memory associated therewith, and performing a traceback on the set of accumulated path decisions,

wherein an ACS data path is widened to receive a Yamamoto quality flag for determining whether an encoded frame contains an error or for use in subsequent quality processing.

2. The decoder system of claim 1, further including a widened state metric memory for processing the Yamamoto quality flag from the widened ACS data path.

3. The decoder system of claim 2, wherein the Yamamoto quality flag is determined by comparing a path difference to a predetermined threshold.

4. A decoder system, comprising:

a State Metric Update unit including a state metric memory and a cascaded Add/Compare/Select (ACS) unit,

wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory,

wherein an ACS stage is operable to identify a plurality of path decisions and communicate the identified path decisions to a next ACS stage coupled thereto; and

a Traceback unit for storing a set of accumulated path decisions in a traceback memory associated therewith, and performing a traceback on the set of accumulated path decisions,

wherein at least one of the ACS stages is padded to enable traceback operations on data frames having differing sizes.

5. The decoder system of claim 4, wherein the at least one ACS stages is padded *via* a modified ACS operation.

6. The decoder system of claim 5, wherein the modified ACS operation comprises forcing a selection of a top butterfly node so that traceback may occur from a desired state of zero.

7. The decoder system of claim 5, wherein the modified ACS operation comprises forcing a selection of a top and bottom butterfly node so that traceback may occur from any desired state.

8. The decoder system of claim 5, wherein the modified ACS operation comprises forcing a new state metric value equal to a prior state metric value so that state metric values are preserved at the end of the data frame.

9. The decoder system of claim 5, wherein the modified ACS operation is communicated to the at least one ACS stages *via* a code associated with a branch metric for the at least one ACS stage.

10. The decoder system of claim 5, wherein the modified ACS operation is communicated to the at least one ACS stages *via* a signal associated with the decoder system.

11. A decoder system, comprising:

a State Metric Update unit including a state metric memory and a cascaded Add/Compare/Select (ACS) unit,

wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory,

wherein an ACS stage is operable to identify a plurality of path differences and communicate the identified path differences to a next ACS stage coupled thereto; and

a Traceback unit for storing a set of accumulated path decisions in a traceback memory associated therewith, and performing a traceback on the set of accumulated path decisions,

wherein the path decisions associated with the ACS stage and the next ACS stage are accumulated as a set during the ACS operations before being written to the traceback memory, thereby minimizing accesses to the traceback memory,

wherein the path differences associated with the ACS stage and the next ACS stage provide a reliability estimation of the correctness of the path decisions.

12. The decoder system of claim 11, wherein the ACS stage is operable to identify the path decisions by utilizing the path differences.

13. The decoder system of claim 11, wherein the identified path differences are accumulated as a set by forwarding the identified path differences from the ACS stage to the next ACS stage during ACS operations.

14. The decoder system of claim 13, wherein the identified path differences are accumulated as a set by widening an ACS data path to receive the identified path differences from the ACS stage and forwarding the identified path differences to the next ACS stage.

15. The decoder system of claim 14, wherein the accumulated set of path differences are routed from the ACS stage into a path selection circuit within the next ACS stage.

16. The decoder system of claim 15, wherein the path selection circuit is operable to accumulate the identified path differences by combining the identified path differences from the ACS stage with identified path differences from the next ACS stage.

17. The decoder system of claim 16, wherein the combined identified path differences are maintained in the widened ACS data path.

18. The decoder circuit of claim 15, wherein the path selection circuit further comprises at least one multiplexor for selecting and routing identified path differences to the next ACS stage, and at least one appending circuit for combining path differences from the ACS stage with the identified path differences from the next ACS stage.

19. The decoder system of claim 11, wherein the path differences and path decisions are stored in memory, wherein an address portion associated with the path difference relates to an address portion associated with the path

decisions, wherein the associated address portion of the path differences are utilized to retrieve the path decisions stored in memory.

20. The decoder system of claim 11, wherein the path differences and path decisions are stored in memory, wherein an address portion associated with the path difference relates to an address portion associated with the path decisions, wherein the associated address portion of the path decisions are utilized to retrieve the path differences stored in memory.

21. A decoder system, comprising:

a State Metric Update unit including a state metric memory and a cascaded Add/Compare/Select (ACS) unit; and

an address generation circuit associated with the ACS unit operative to receive control inputs and generate addresses to control the ACS unit over multiple stages of a trellis;

wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory.

22. The decoder system of claim 21, wherein the address generation circuit is utilized for at least one of read and write operations over multiple stages of the trellis.

23. The decoder system of claim 22 further including controllable counters for address generation.

24. The decoder system of claim 22 further including a toggle circuit to differentiate nodes of a trellis.

25. The decoder system of claim 22 further including at least one of a phase A operation for reads and a phase B operation for reads.

26. The decoder system of claim 22 further including at least one of a phase A operation for writes and a phase B operation for writes.

27. A decoder system, comprising:

a State Metric Update unit including a state metric memory and a cascaded Add/Compare/Select (ACS) unit; and

an index generation circuit associated with the ACS unit operative to receive control inputs and generate indices to control the ACS unit over multiple stages of a trellis;

wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory.

28. The decoder system of claim 27, wherein the index generation circuit is utilized for at least one of read and write operations over multiple stages of the trellis.

29. The decoder system of claim 27, further including controllable counters for index generation.

30. The decoder system of claim 27, further including a toggle circuit to differentiate nodes of a trellis.

31. The decoder system of claim 27, further including at least one of a phase A operation for reads and a phase B operation for reads.

32. The decoder system of claim 27, further including at least one of a phase A operation for writes and a phase B operation for writes.

33. A decoder system, comprising:

a State Metric Update unit including a state metric memory and a cascaded Add/Compare/Select (ACS) unit; and

an address and index generation circuit associated with the ACS unit operative to receive control inputs and generate addresses and indices to control the ACS unit over multiple stages of a trellis;

wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory.

34. The decoder system of claim 33, wherein the address and index generation circuit is utilized for at least one of read and write operations over multiple stages of the trellis.

35. A method for Viterbi decoding, comprising the steps of:

providing a State Metric Update unit including a state metric memory;

providing a cascaded Add/Compare/Select (ACS) unit;

wherein the cascaded ACS unit comprises a plurality of serially coupled ACS stages for performing a plurality of ACS operations in conjunction with the state metric memory,

identifying a plurality of path decisions and path differences;

communicating the identified path decisions and the identified path differences to a next ACS stage coupled thereto;

providing a Traceback unit for storing a set of accumulated path decisions in a traceback memory associated therewith; and

performing a traceback on the set of accumulated path decisions;

wherein the path decisions associated with the ACS stage and the next ACS stage are accumulated as a set during the ACS operations before being written to the traceback memory, thereby minimizing accesses to the traceback memory,

wherein the path differences associated with the ACS stage and the next ACS stage provide a reliability estimation of the correctness of the path decisions.

36. The method of claim 35, wherein the identified path differences are accumulated as a set by including the step of forwarding the identified path differences from the ACS stage to the next ACS stage during ACS operations.

37. The method of claim 36, wherein the identified path differences are accumulated as a set by including the steps of:

widening an ACS data path to receive the identified path differences from the ACS stage; and

forwarding the identified path differences to the next ACS stage.

38. The method of claim 37, further including the step of including a Yamamoto quality flag in the widened ACS for determining whether an encoded frame contains an error or for use in subsequent quality processing.